

REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 50-71 are pending in this case. Claims 50, 58, 64, and 70 are amended by the present amendment. Amended Claims 50, 58, 64, and 70 are supported by the specification¹ and original claims. Amended Claims 50, 58, 64, and 70 add no new matter.

In the outstanding Official Action, Claims 53, 61, and 67 were objected to for informalities. Claims 50-69 were rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement and written description requirements. Claims 50-69 were rejected under 35 U.S.C. §112, second paragraph, as indefinite. Claims 70 and 71 were rejected under 35 U.S.C. §102(b) as anticipated by Read et al. (U.S. Patent No. 5,420,809, herein "Read"). Claims 50-53, 55-61, 63-67, and 69 were rejected under 35 U.S.C. §103(a) as unpatentable over Read in view of Davidson et al. (U.S. Patent No. 5,613,157, herein "Davidson"). Claims 54, 62, and 68 were rejected under 35 U.S.C. §103(a) as unpatentable over Read in view of Davidson and further in view of Short (*Embedded Microprocessor Systems Design: An Introduction Using the Intel 80C188EB*, herein "Short").

An interview was held on November 22, 2004 to discuss the present case, attended by Examiner Li, Ed Tracy, and Surinder Sachar. The applicants would like to thank the Examiner for her time in conducting the interview. During the interview, differences between the claims and the cited references were discussed in detail, and claim amendments were discussed to address interpretations of the claims with respect to the teachings of the cited art.

¹See e.g. Specification at page 52, lines 7-20 and page 86, lines 2-10.

In response to the objection to Claims 53, 61, and 67, the objection is noted by the applicants. However, the order of the claims has not been changed in accordance with MPEP §608.01(m). Accordingly, the objection is believed to be overcome.

In response to the rejection of Claims 50-69 under 35 U.S.C. §112, first paragraph, it is respectfully submitted that Claims 50-69 are enabled by the original specification. The Background discusses the problem in the art that the conventional systems did not allow upgrade of the system by the replacement of a single unit.² The inventors discovered that this problem could be solved by making the image processing unit a SIMD processing unit. The other units could then be manufactured as independent, replaceable units.

The Specification further states that an embodiment of the invention includes an image reading unit and/or an image data unit and/or an image memory control unit and/or an image processing unit and/or an image writing unit and/or a facsimile control unit structured as independent units at page 86, lines 2-24. Accordingly, it is respectfully submitted that one having ordinary skill in the art could make or use the inventions recited in Claims 50-69. Thus, it is respectfully submitted that Claims 50-69 are in compliance with all requirements under 35 U.S.C. §112, first paragraph.

With regard to the rejection of Claims 50-69 under 35 U.S.C. §112, second paragraph, Claim 50 is amended to recite “the image processing unit is configured to perform image processing” rather than “the image processing unit is configured to perform the image processing.” Claims 50, 58, 64, and 70 are amended to recite “a same instruction of said second parallel processing job” rather than “a same second parallel processing job instruction.” Accordingly, it is respectfully submitted that Claims 50-69 are in compliance with all requirements under 35 U.S.C. §112, second paragraph.

²See Specification at page 8, line 7 to page 9, line 23.

With regard to the rejection of Claim 70 under 35 U.S.C. §102(b) as anticipated by Read, that rejection is respectfully traversed.

Amended Claim 70 recites a multi-function image processing apparatus comprising
inter alia:

an image reader configured to read first image data, said image reader including at least one processor;

an image writer configured to image data onto a transcription sheet, said image writer including at least one processor;

an image processing unit configured to process the first image data to second image data and transmit the second image data to the image writer, said image processing unit including at least one processor; and

a facsimile control unit configured to transmit the first data read by the image reader as a facsimile image and receive facsimile image data, said facsimile control unit including at least one processor,

wherein said multi-function image processing apparatus is configured to operate a first parallel processing job comprising a printing, copying, or facsimile job and a second parallel processing job comprising a printing, copying, or facsimile job by having a processor of one of said image reader, said image writer, said image processing unit, and said facsimile control unit operating said first parallel job and a processor of one of said image reader, said image writer, said image processing unit, and said facsimile control unit operating said second parallel job, said first and said second parallel processing jobs operating on processors of different ones of said image reader, said image writer, said image processing unit, and said facsimile control unit at a same time, said printing job is operated by the image processing unit then the image writer, said copying job is operated by the image reader, then the image processing unit, then the image writer, an incoming facsimile job is operated by the facsimile control unit, then the image processing unit, then the image writer, and an outgoing facsimile job is operated by the image reading unit, then the image processing unit, and then the facsimile control unit, the image reader is configured to read data for copying and facsimile functions, the image processing unit is configured to perform the image processing for printing, copying, and facsimile functions, and the image writer is configured to image data on the transcription sheet for printing, copying, and facsimile functions,

...

Read discloses a method of operating a data processing apparatus to compute correlation. Although Read discloses that the data processing apparatus can have facsimile, copying, and printing capability³, it is respectfully submitted that Read does not teach that the apparatus includes an image reader, an image writer, an image processing unit, and a facsimile control unit each with at least one processor, and further that the apparatus operates a first and a second parallel processing job on processors of different ones of the image reader, the image writer, the image processing unit, and the facsimile control unit at the same time, as recited in Claim 70. Accordingly, it is respectfully submitted that Claim 70, and Claim 71 dependent therefrom, is not anticipated by Read and is patentable thereover.

With respect to the rejection of Claim 50 as unpatentable over Read in view of Davidson, the rejection is respectfully traversed.

Amended Claim 50 recites a multi-function image processing apparatus comprising
inter alia:

...
an input unit configured to input an interruption request to interrupt a first parallel processing job performed by the parallel processing unit in favor of a second parallel processing job, said first parallel processing job comprising a printing, copying, or facsimile job and said second parallel processing job comprising a printing, copying, or facsimile job;
...

As stated above, Read discloses a method of operating a data processing apparatus to compute correlation. Although Read discloses a TASK interrupt flag configured to switch a task of a digital image/graphics processor upon receipt of the interrupt from a master processor⁴, there is no teaching or suggestion in Read that a first parallel processing job is a printing, copying, or facsimile job and the second parallel processing job is a printing, copying, or facsimile job, as recited in Claim 50.

³See Read column 176, line 61 to column 177, line 25.

⁴See Read column 106, lines 53-60.

Davidson discloses an address range extension for a modular computer. It is respectfully submitted that there is no teaching or suggestion in Davidson for an input unit configured to input an interruption request to interrupt a first parallel processing job performed by a parallel processing unit in favor of a second parallel processing job, the first parallel processing job comprising a printing, copying, or facsimile job and the second parallel processing job comprising a printing, copying, or facsimile job, as recited in Claim 50.

Since the cited references do not teach or suggest each and every element of Claim 50, it is respectfully submitted that Claim 50, and Claims 51-57 dependent therefrom, is patentable over the cited references.

Amended independent Claims 58 and 64 recite similar elements to Claim 50. It is respectfully submitted that Claims 58 and 64, and Claims 59-63 and 65-69 dependent therefrom, are patentable over the cited art for the reasons discussed above with respect to Claim 50.

Accordingly, the pending claims are believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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